Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims:

1. (currently amended) A method of making a multi-layered storage structure, comprising:

forming a device layer on a single-crystal wafer;

cleaving the device layer from the wafer;

repeating the forming and cleaving to provide a plurality of cleaved device layers; ~~and~~

bonding the cleaved device layers together to form the multi-layered storage structure; and

forming a three-dimensional cross-point array memory structure using the bonded device layers.

2. (original) The method of claim 1, wherein the forming comprises implanting devices on the wafer.

3. (original) The method of claim 1, wherein the forming comprises forming a device layer comprising devices selected from the group consisting of diodes, transistors, antifuses, and tunnel junctions.

4. (currently amended) ~~The method of claim 1,~~ A method of making a multi-layered storage structure, comprising:

forming a device layer on a single-crystal wafer;

cleaving the device layer from the wafer;

repeating the forming and cleaving to provide a plurality of cleaved device layers; and

bonding the cleaved device layers together to form the multi-layered storage structure, wherein the forming comprises forming a device layer comprising vertical diodes; further wherein the storage structure is a vertical memory structure.

5. (currently amended) The method of claim 1, wherein the repeating comprises forming the plurality of cleaved device layers from the same single-crystal ~~silicon~~ wafer.

6. (original) The method of claim 1, wherein the bonding comprises plasma-activated bonding.

7. (canceled)

8. (original) The method of claim 1, wherein the cleaving comprises ion-implantation induced layer splitting of the wafer.

9. (original) The method of claim 1, wherein the cleaving comprises anodic etching and annealing of the wafer.

10. (original) The method of claim 1, wherein the storage structure comprises memory or a processor.

11. (withdrawn) A cross-point memory structure, comprising:

crystalline isolated diode pillars formed from a cleaved wafer layer;

row lines crossing the crystalline isolated diode pillars; and

column lines crossing the crystalline isolated diode pillars and the row lines.

12. (withdrawn) The structure of claim 11, wherein the diode pillars are together cleaved from the wafer in a layer, the layer being applied next to the row lines.

13. (withdrawn) The structure of claim 11, wherein the diode pillars comprise Schottky diodes.

14. (withdrawn) The structure of claim 11, wherein the diode pillars comprise diodes selected from the group consisting of P-N diodes and PIN diodes.

15. (withdrawn) The structure of claim 11, further comprising an antiferromagnetic layer applied between the diode pillars and the column lines.

16. (withdrawn) The structure of claim 11, further comprising a storage layer applied between the row lines and the diode pillars.

17. (withdrawn) The structure of claim 11, wherein the memory structure comprises magnetic memory.

18. (withdrawn) A method of making a cross-point array structure, comprising:

patterning a single-crystal silicon wafer;

cleaving a layer from the patterned wafer; and

applying the cleaved layer over conductive traces.

19. (withdrawn) The method of claim 18, wherein the layer is a P-N layer.

20. (withdrawn) The method of claim 18, further comprising etching the layer to create a plurality of vertical diodes in communication with the conductive traces.

21. (withdrawn) The method of claim 18, wherein the conductive traces are first conductive traces, the method further comprising forming second conductive traces over the cleaved layer.

22. (withdrawn) The method of claim 21, further comprising using the second conductive traces in masking and patterning the cleaved layer.

23. (withdrawn) A memory stack comprising a plurality of bonded memory layers, each memory layer being cleaved from a single-crystal silicon wafer.

24. (withdrawn) The memory stack of claim 23, wherein the memory layers each comprise devices selected from the group consisting of diodes, transistors, antifuses, and tunnel junctions.

25. (withdrawn) The memory stack of claim 23, wherein the memory layers comprise vertical diodes.

26. (withdrawn) Apparatus for making a cross-point array structure, comprising:

means for patterning a single-crystal silicon wafer;

means for cleaving a layer from the patterned wafer; and

means for applying the cleaved layer over conductive traces.

27. (withdrawn) The apparatus of claim 26, further comprising means for etching the layer to create a plurality of vertical diodes in communication with the conductive traces.

28. (withdrawn) The apparatus of claim 26, wherein the conductive traces are first conductive traces, the apparatus further comprising means for forming second conductive traces over the cleaved layer.

29. (new) A method of making a multi-layered storage structure, comprising:

forming a first device layer on a semiconductor substrate;

cleaving, from the substrate, the first device layer and a first substrate section, the first substrate section being below the first device layer and including a first portion of the substrate;

forming a second device layer on the substrate;

cleaving, from the substrate, the second device layer and a second substrate section, the second substrate section being below the second device layer and including a second portion of the substrate; and

bonding the first and second device layers to form the multi-layered storage structure.

30. (new) The method of claim 29 further comprising forming diodes on the first and second device layers.

31. (new) The method of claim 29 further comprising forming a magnetic memory structure on the first and second device layers.

32. (new) The method of claim 29 further comprising planarizing surfaces of the first and second substrate sections before bonding the first and second device layers.

33. (new) The method of claim 29 further comprising polishing surfaces of the first and second substrate sections to define metal interconnection patterns before bonding the first and second device layers.

34. (new) The method of claim 29, wherein the multi-layered storage structure is a vertical memory structure.

35. (new) The method of claim 29 further comprising forming a three-dimensional cross-point array memory structure with the first and second device layers.